B6 The method according to claim 19 wherein said single substrate is a sapphire substrate.

Remarks

Applicant hereby respectfully requests that the above-identified co-pending parent application (Serial No. 09/517,292) be amended as indicated. The present application is a divisional application of this co-pending application. In this divisional application, method claims are presented pertaining to the invention of parent application Serial Number 09/517,292.

By this amendment, Applicant has amended the disclosure to be one and the same as the parent application as amended. An additional amendment has been made to the disclosure to correct a typographical error not previously found. This typographical error lies on page 9, in the paragraph starting at line 15. Original method claims are hereby presented. One of these method claims has been amended by this preliminary amendment to provide consistency with the description and drawings. Additional method claims are also presented. Claims 1-11 and 19-20 should remain in the application.

Any inquiry concerning this case should be directed to Applicant's attorney, Mr. Peter Lipovsky at (619) 553-3001.

Respectfully submitted,

by Peter A. Lipovsky

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28 February 2002
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Navy Case No. 83730

37 CFR 1.121(b)(2) ATTACHMENT

In the Description:

On page 1, between lines 3 and 4, please insert the following:

CROSS-REFERENCE TO RELATED APPLICATION

This application is a division of United States Patent Application Serial Number 09/517.292 filed 2 March 2000.

The paragraph starting on page 3, line 5:

Most of the development of bipolar junction transistors of silicon-on-sapphire has been concentrated in the area of lateral bipolar junction transistors, epitaxial vertical bipolar junction transistors, and heteroepitaxy bipolar junction transistors. This work has been recorded respectively by P.K. Vasudev in his article in the IEEE Circuits and Devices magazine titled: Recent Advances in Solid-Phase Epitaxial Recrystalization of SOS with Applications to CMOS and Bipolar Devices, of July 1987, pp. 17-19: by F.P. Heiman and P.H. Robinson in their article in *Solid State Electronics* titled: Silicon-on-Sapphire Epitaxial Bipolar Transistors of 1968, Volume 11, pp. 411-418; and by E.N. Cartagena, B.W. Offord and G. Garcia in their article in *Electronics Letters* titled: Bipolar Junction Transistors Fabricated in Silicon-on-Sapphire of 1992, Volume 28, pp. 983-985.

The paragraph starting on page 6, line 19:

Referring to FIGS. 1A and 1B, cross-sectional views of complimentary vertical bipolar

junction transistors 10 fabricated of silicon-on-sapphire according to the invention [is] are shown. The elements of these transistors will be discussed first. Following this will be a discussion of the steps used to fabricate these transistors.

The paragraph starting on page 9, line 15:

FIG. 9 illustrates a process used to create an N+ region in wafer 34 that is part of sub-collector region 26 of NPN vertical transistor 14 illustrated in FIG. 1. Photoresist layer 56 is produced by coating all of wafer 34 with photoresist and selectively removing the resist from certain regions of the wafer as is well-known to those knowledgeable in the art of semiconductor processing. Implantation to form the N+ region may utilize arsenic (As) ions for example at 80 KeV at a [does] dose of $3x10^{15}$ ions/cm^2. Photoresist layer 56 prevents the ions from penetrating into region 58. However the As ions readily penetrate into region 60 of wafer 34.

Please amend the claims as follows:

CLAIM 8 (amended)

The method of claim 1 further including the steps of:

forming a P+ collector [plugs] plug region in said N base region for said PNP transistor so that said P+ collector [plugs are] plug region is incorporated into said P+ collector for said PNP transistor;

forming an N+ collector plug [regions] region in said [N collector region] P intrinsic base

region for said NPN transistor so that said N+ collector [plugs are] plug region is incorporated into said N collector region of said N+ sub-collector region for said NPN transistor;

forming individual conductive metal contacts with said collector plug regions; and

forming an oxide region between said collector plug metal contacts.